

TSMC-02-115/320

April 30, 2004

To: Commissioner for Patents  
P.O.Box 1450  
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572  
28 Davis Avenue  
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/785,522 02/24/04 |

Yue-Der Chih

AN ARRAY STRUCTURE OF TWO-TRANSISTOR  
CELLS WITH MERGED FLOATING GATES FOR  
BYTE ERASE AND RE-WRITE IF DISTURBED  
ALGORITHM

#### INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56.

#### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being  
deposited with the United States Postal Service as first class  
mail in an envelope addressed to: Commissioner for Patents,  
P.O. Box 1450, Alexandria, VA 22313-1450, on May 4, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

Stephen B. Ackerman 5/4/04

U.S. Patent 6,376,876 to Shin et al., "NAND-Type Flash Memory Devices and Methods of Fabricating the Same," discusses a NAND type flash memory array that uses a low resistance common source line with low aspect ratio bit line contact holes.

U.S. Patent 6,400,603 to Blyth et al., "Electronically-Eraseable Programmable Read-Only Memory Having Reduced-Page-Size Program and Erase," discusses a flash EEPROM array directed to the reduced size of blocks or pages that are to be erased in a write or an erase operation.

U.S. Patent 6,128,220 to Banyai et al., "Apparatus for Enabling EEPROM Functionality Using a Flash Memory Device," discusses a flash memory device that provides a byte-alterable nonvolatile memory.

U.S. Patent 6,121,087 to Mann et al., "Integrated Circuit Device with Embedded Flash Memory and Method for Manufacturing Same," discloses an integrated circuit device with an embedded EEPROM memory.

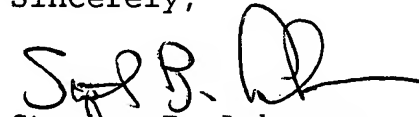
U.S. Patent 6,088,269 to Lambertson, "Compact Page-Erasable EEPROM Non-Volatile Memory," discloses a compact page erasable EEPROM without the use of the control gate to improve electron tunneling efficiency during programming.

U.S. Patent 5,812,452 to Hoang, "Electrically Byte-Selectable and Byte-Alterable Memory Arrays," discloses a byte selectable and byte alterable memory array.

U.S. Patent 5,544,103 to Lambertson, "Compact Page-Erasable EEPROM Non-Volatile Memory," discloses a compact, electrically erasable and programmable nonvolatile memory device which has unique programming and erasing techniques in which the control gate is eliminated as a means for improving electron tunneling efficiency.

U.S. Patent 5,033,023 to Hsia et al., "High Density EEPROM Cell and Process for Making the Cell," discusses an EEPROM directed to a byte erase operation.

Sincerely,

A handwritten signature in black ink, appearing to read "Stephen B. Ackerman", with a stylized flourish extending to the right.

Stephen B. Ackerman,  
Reg. No. 37761

Form PTO-1449

Document Number (Specimen)

Application Number

TSMC-02-115/320

10/785,522

Applicant

Yue-Der Chih

Filing Date

02/24/04

Group 1/1 Unit

INFORMATION DISCLOSURE CITATION  
IN AN APPLICATION

MAY 06 2004

(Use approval sheets if necessary)

## U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	TITLE	CLASS	SUBCLASS	PLUNG DATE IF APPROPRIATE
	63768764	4/23/02	Shin et al.	257	315	10/4/00
	64006036	4/02	Blyth et al.	365	185.12	5/3/00
	6128220	10/3/00	Bangai et al.	365	185.11	1/21/99
	61210879	1/19/00	Mann et al.	438	258	6/18/96
	6088269	7/11/00	Lambertson	365	185.28	11/6/98
	5812452	9/22/98	Hoang	365	185.11	6/30/97
	55441038	6/96	Lambertson	365	185.15	7/12/94
	5033023	7/16/91	Hsia et al.	365	185	4/8/88

## FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

## OTHER DOCUMENTS (Including Author, Title, Date, Portmox Pages, Etc.)


EXAMINER

DATE COMPLETED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.